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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/773,583

Filing Date: February 05, 2004

Appellant(s): LARSON ET AL.

Karen Lenaburg #58571

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/29/2007 appealing from the Office action mailed 12/05/2006.

(1) Real Party in interest

A statement identifying by name the real party interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The statement of the status of amendments contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US 2005/0105350	Zimmerman, David	5-2005
US 6622188	Goodwin et al	9-2003
US 6901494	Zumkehr et al	5-2005
Micron Double Data Rate (DDR) SDRAM	Micron	2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 40-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US 2005/0105350) in view of Zumkehr (US 6901494).

As in claim 40, Zimmerman discloses a method for executing read and write commands in a memory system having a memory bus (Fig 2, par. 17), issuing a read command to access a first memory location in the memory system (Fig 2, par. 3 host and controller accesses/read data in memory SDRAM); retrieving read data from the first memory location (Fig 2, par. 3 and 14, a first data is read from a first location of device DRAM); receiving the read data on the bidirectional memory bus from the memory system (Fig 2, par. 3 and 14, a first data is read from a first location of device DRAM from module 120); and providing the write data to the memory bus (Fig 2, par. 3 and 14, write a second data to a second location of device DRAM via 112 122).

Zimmerman does not expressly disclose the claim's bidirectional. However, Goodwin discloses a mechanism in which multiple memory devices, i.e expansion devices are connected to a bidirectional bus as shown in Goodwin's Fig 2. It would have been obvious to one of ordinary skill in the art at the time of invention to include bi directional bus as suggested by Goodwin in Zimmerman's system thereby further allows read and write data in the devices to be transferred effectively over the same bidirectional data bus (Goodwin's column 1 lines 10-35). Zimmerman and Goodwin do not expressly disclose the claim's details associating to scheduling a write command after a read command and bypassing data. However, Zumkehr discloses before completion of the read command, scheduling a write command to write data to a second memory location in the memory system (col. 3 lines 40-50, the pipeline of operations means that a subsequent command is scheduled even before completion of a previous command); prior to receiving the read data on the memory bus from the memory

system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system (col. 3 lines 40-50, the pipeline of a write command means write data is provided even before completion of a previous command; Fig 5A and 5B show examples of a read command and a write command both requesting large burst of data. A scenario based on Fig 5B comprise a read command follows by a write command of small amount of data, for example one clock cycle of data, can be as followed:

Examiner note: the Fig 5A and 5B illustrates the access to memory device with a **latency** of 3 clocks, i.e time delay from issuing the read command to SDRAMs memory devices at the third clock, i.e Fig 5B shows as a read command from hub to sdram at T2B first block, to the read data returning by the SDRAMs of the memory system at the sixth clocks. Of course, the actual latency value can be larger and as such write command and/or additional write data can be pipelined/ provided to memory system during this latency time/window, before the read data returning by the memory system to the controller. Examiner note: definition of latency of memory is commonly known and defined as time from the read command issues to the memory device until the memory device return the read data, see micron page 13. Micron teaches that the read latency is based on delay time TRCD time which can be mapped into several clocks cycles.

This definition of latency is consistent with the definition provided by Applicant who states " **..the latency problem...** More specifically, when a memory device read command is coupled to a system memory device, such as a synchronous DRAM

("SDRAM") device, **the read data are output from the SDRAM device only after a delay of several clock periods.** Therefore, although SDRAM devices can synchronously output burst data at a high data rate, **the delay in initially providing the data** can significantly slow the operating speed of a computer system using such SDRAM devices", see specification's page 2 lines 16-24.

Therefore assuming a device with a read latency of 5 clocks and using the timing based on Fig 2B, a read command at clock 1, i.e T1B first block, which means the corresponding read data is not returning until at least the eight clock cycle, i.e at T4B first block. This is a large timing window which certainly large enough to allow two write commands in a pipeline manner on the rambus at the second clock and third clock on the rambus and two corresponding data respectively on the sdram data bus at clock 5 and 6. The arrival of second write command pushing/allowing the first write data corresponding to the first write command to SDRAM at clock 6, i.e T3B first block. Because the read data is not returned at least until the clock 8, therefore it's clear that the first write data is provided prior to receiving the read data as recited in the claim's limitation).

Zumkehr further discloses in the system memory, bypassing the read data on the bidirectional memory bus (Fig 3. col. 5 lines 35-45, shows data is stored in write-buffer 330 thus allowing read data 340 going through);

It would have been obvious to one of ordinary skill in the art at the time of invention to include the memory controller hub circuits and methods as suggested by Zumkehr in Zimmerman's system to allow transferring read data while temporary storing

write data, thereby resulting in more efficiently usage of the memory bus in the system (Zumkehr's column 6 lines 35-60; read and write data transferring through the same bidirectional data bus Fig 3: #350 data signals).

As in claim 41, Zimmerman and Goodwin do not expressly disclose the claim's bypass. However, Zumkehr further discloses wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus (col. 5 lines 35-45, Fig 3, data is stored in write-buffer 330 thus allowing read data 340 going through). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt the teaching of Zumkehr in Zimmerman's system modified by Goodwin for the same reasons stated above.

As in claim 42, Zimmerman and Goodwin do not expressly disclose the claim's bypass. However, Zumkehr further discloses temporarily storing the write data in a bypass buffer during the receipt of the read data (col. 5 lines 35-45, Fig 3, data is stored in write-buffer 330 thus allowing read data 340 going through). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt the teaching of Zumkehr in Zimmerman's system modified by Goodwin for the same reasons stated above.

As in claim 43, Zimmerman discloses wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system (Fig 2 write data must go through memory module 130). Zimmerman and Goodwin do not expressly disclose the claim's decoupling. However,

Zumkehr further discloses write data is going through a hub/translation hub (Fig 2 220) before decoupling the write data from the memory bus (Figs 2 and 3, write data is stored/decoupling from the memory bus). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt the teaching of Zumkehr in Zimmerman's system modified by Goodwin for the same reasons stated above.

(10) Response to Argument

Appellant's arguments in response to the last office action have been fully considered but they are not persuasive. Examiner respectfully traverses Appellant's arguments for the following reasons:

A) Appellant's arguments regarding the rejection of claim 40 under U.S.C 35 103(a) have been fully considered but they are not persuasive.

A0) Appellant argues that the cited references do not teach "the data bypass capabilities when a read command is issued, and before the **read latency** is met, **issuing** a write command and corresponding write data".

Examiner contends that Appellant is arguing limitations that are not in the claims. The read latency of a memory device that Appellant referring to in his argument, is well known in the art and it means the time period of several clock cycles, from the memory device received the read command (at the first clock cycle) until it provides the beginning of read data (at the n clock cycle. Data continues to be transferred in additional clock cycles, then the execution of the read command is completed). The

present invention does not claim or have any limitation regarding read latency and/or requiring "issuing of a subsequent write command and before the **read latency** is met" as argued. Instead the claim 40 recites "before completion of the read command, scheduling a write command..". Scheduling a write command indicates the intention to issue a write command at any time subsequently. In other words, **the scheduling event of a write command is not the same as the issuing event of a write command**, and the issuing of the write command can be issued any time subsequently. Thus claim 40 intends to cover a much broader period of time that allowing the write command to be issued, much longer than the "before read latency is met" period. In fact, Appellant does not have any "read latency" limitation recited in the claim, perhaps and conveniently to cover a time period larger that the "read latency" period.

As discussed above, Appellant is arguing limitations that are not in the claims, this is a frivolous argument, and therefore the argument is not persuasive.

Claim 40 at best, as a whole, describes the overlapping of a read command operation and a subsequent write command operation, wherein the write command can be issued anytime during and **before the read command operation is completed**, as discussed above.

Specifically, claim 40 describes before the read command operation is completed, then scheduling a write command to write data ("before completion of the read command, schedule a write command.."), and only requires "receiving the read data on the bidirectional memory bus from the memory system; and providing the write data to the bidirectional memory bus".

Thus at best, the recited claim is interpreted such that when a write command is issued, in a pipelining manner, at a time between a read command is issued (by the memory controller) and the time the read data completely arrived at the memory controller, this write command would meet the limitations recited in the claim.

Zumkehr teaches such memory system as shown in Fig 5B. As stated in the rejection of claim 40, a scenario based on Zumkehr Fig 5B timing diagram that teaches "prior to receiving the read data on the memory bus providing a write data ..providing write data corresponding to the write command.." , wherein a read command follows by a write command of small amount of data, for example one clock cycle of data, can be as followed:

Examiner note: the Fig 5A and 5B illustrates the access to memory with a **latency** of 3 clocks, i.e time delay from issuing the read command to SDRAMs memory devices at the third clock, i.e read command from hub to sdram at T2B first block, to the read data returning by the SDRAMs of the memory system at the sixth clocks. Of course, the actual latency value can be larger and as such additional write commands and/or additional write data can be pipelined/ provided to memory system during this latency time/window before the read data returning by the memory system to the controller. Examiner note: definition of latency of memory is commonly known and defined as time from the read command issues to the memory device until the memory device return the read data, see micron. Micron teaches that the read latency is based on delay time TRCD time which can be mapped into several clocks cycles.

This definition of latency is consistent with the definition provided by Applicant who states " **..the latency problem...** More specifically, when a memory device read command is coupled to a system memory device, such as a synchronous DRAM ("SDRAM") device, **the read data are output from the SDRAM device only after a delay of several clock periods.** Therefore, although SDRAM devices can synchronously output burst data at a high data rate, **the delay in initially providing the data** can significantly slow the operating speed of a computer system using such SDRAM devices", see specification's page 2 lines 16-24.

Therefore assuming a device with a read latency of 5 clocks and using the timing based on Fig 2B, a read command at clock 1, i.e T1B first block, which means the corresponding read data is not returning until at least the eight clock cycle, i.e at T4B first block. This is a large timing window which certainly large enough to allow two write commands in a pipeline manner on the rambus at the second clock and third clock on the rambus and two corresponding data respectively on the sdram data bus at clock 5 and 6. The arrival of second write command pushing/allowing the first write data corresponding to the first write command to SDRAM at clock 6, i.e T3B first block. Because the read data is not returned at least until the clock 8, therefore it's clear that the first write data is provided prior to receiving the read data as recited in the claim's limitation.

In other words, because the read latency is several cycles, a large timing window, that sufficiently allows two write commands including sending data of a write command in the bypass buffer to memory device as required in the claim.

Examiner submits that the above scenario of Zumkehr is sufficiently to teach the main Applicant's argument that Zumkehr does not teach "...a write data can not be provided prior to receiving the read data.."

A1) Regarding Appellant's arguments of item D in the Appeal Brief,

First, Appellant continues to argue about the "read latency" that is not in the claim, as discussed in item A0 above;

Second, Examiner contents that Appellant mischaracterize Zumkehr's teaching regarding the "read latency".

Appellant argues "...In contrast, Fig 5B, which includes a write buffer in the translator hub, shows that a new write command 520B following a read command 501B can be issued before the read latency of the previously issued read command 501B is met....However, the write data 527B associated with the new write command 530B remains in the memory and cannot be issued until *after* the read latency of the previously issued read command 501B is met.." and Appellant concludes "Therefore, the Zumkehr reference does not disclose or fairly suggest data bypass capabilities when a read command is issued, and before the read latency is met, issuing a write command and corresponding write (sic).

It's not clear what "issuing a write command and corresponding write" means. Examiner assumes that Appellant intends to state "issuing a write command and corresponding write data". Thus apparently Appellant misinterprets Zumkehr's teaching of the read latency value being used for write commands, and thereby Appellant further asserting that the subsequent write command and corresponding write

command must occur before the ending of the previous read command operation.

Although Examiner does not agree with Appellant's assertion and the mischaracterization of Zumkehr's teaching, Zumkehr's teaching of read latency and providing the corresponding write data before the read data as recited in the claim is discussed in details in item A0 above.

Finally, Applicant point to Zumkehr's col. 4 lines 45-68 to col. 5 lines 1-23, Zumkehr "read latency" time period is referred to be used by specific memory controller logic so that it can pace apart sending out subsequent command operations. Thus this pacing time period may be arbitrary chosen mainly to satisfy pacing requirement of a specific controller/protocol (Rambus memory controller protocol). Realizing that for an actual write operation of a memory device, for example SDRAM memory device, this "read latency" period is not necessary. Zumkehr teaches of using temporary buffering of write data and bypassing circuitry such that read data and write data of several read and write operations can be bypassing and operate in a concurrently manner. By combining with pipelining, this pacing period can be eliminated completely (Zumkehr's column 2 line 61 to column 3 line 50 further teaches that this pacing delay/defer timing requirement ("read latency") for the write operation of a specific memory controller can be reduced and eliminated (i.e met, no longer required). In other words, Zumkehr teaches that by pipelining several read and write commands/operations, and providing buffers to temporary storing write commands and their associating data, such that these write commands and their data can be written concurrently to multiple memory devices, thereby effectively, the pacing time period is

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eliminated. Zumkehr's teaching of buffering data for bypassing data can be readily applied to any system memory, and any memory devices, and memory controllers, see Zumkehr's column 3 lines 35 to 50.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/ Duc T. Doan/

Duc T. Doan

Examiner

Art Unit 2188

/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2117

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Supervisory Patent Examiner, Art Unit 2185